voltage so as to provide a first voltage to said word driver circuit;

wherein the amplitude of said first voltage is larger than that of said operating voltage so that said word driver circuit can provide the output voltage whose is larger than an amplitude of an input voltage;

wherein said voltage generator circuit provides a small output current to said word driver circuit in order to compensate for a leakage current and said voltage generator circuit provides a large output current to said word driver circuit in response to a first signal from an outside chip.--

--22. The semiconductor memory according to claim 21, wherein said voltage generator circuit includes

a first circuit supplied with an operating voltage so as to provide a first voltage to said word driver circuit; and

a second circuit supplied with the operating voltage so as to provide the first voltage to said word driver circuit;

wherein said first circuit provides the first voltage in response to a first signal from outside chip;

wherein said second circuit provides the first voltage to said word driver circuit in order to compensate for a leakage current while said first circuit stops providing the first voltage to said word driver circuit.--

~~23~~ 3. The semiconductor memory according to claim ~~21~~ 1, wherein said voltage generator circuit has a clamp circuit to thereby clamp the first voltage to a predetermined voltage.--

--24. The semiconductor memory according to ~~claim 23~~, wherein said second circuit has a detector circuit which provides a signal to make said second circuit stop providing said first voltage when the first voltage is larger than the predetermined voltage.--

~~25~~ 5. The semiconductor memory according to claim ~~21~~ 1, wherein said first signal is a row address strobe signal.--

~~26~~ 6. The semiconductor memory according to claim ~~21~~ 1, wherein said semiconductor memory is a dynamic random access memory.--

~~27~~ 7. The semiconductor memory according to claim 21, wherein said semiconductor memory is a static random access memory.--

REMARKS

The specification has been amended to correct all errors previously corrected by amendments in the parent application.

Fig. 52 of the drawings has been re-numbered Fig. 52A and 52B and new drawings of Figs. 1, 52A & 52B, 55-57, 61, 64, 66, 69, and 70 are attached for the Examiner's approval.

Claims 1-20 have been cancelled and new claims 21-27 were added.